

Day : Monday  
Date: 5/23/2005

Time: 10:18:09

 PALM INTRANET**Inventor Name Search Result**

Your Search was:

Last Name = LI

First Name = LI

Application#	Patent#	Status	Date Filed	Title	Inventor Name 42
<a href="#">60660475</a>	Not Issued	020	03/10/2005	BIPHENYL COMPOUNDS USEFUL AS MUSCARINIC RECEPTOR ANTAGONISTS	LI, LI
<a href="#">60646610</a>	Not Issued	020	01/26/2005	USE OF SFRPS AS MARKERS OF BMP ACTIVITY	LI, LI
<a href="#">60646515</a>	Not Issued	020	01/25/2005	THIN FILM OPTICAL DEVICES AND A METHOD OF MANUFACTURING SUCH DEVICES	LI, LI
<a href="#">60361833</a>	Not Issued	159	03/05/2002	NADP-DEPENDENT MALIC ENZYME-LIKE PROTEINS, DERIVED PEPTIDES, AND NUCLEIC ACIDS ENCODING SAME	LI, LI
<a href="#">60360858</a>	Not Issued	159	03/01/2002	NOVEL ALDOSE REDUCTASE-RELATED PROTEIN-LIKE PROTEINS AND NUCLEIC ACIDS ENCODING SAME	LI, LI
<a href="#">60360830</a>	Not Issued	159	03/01/2002	NOVEL AROMATIC-L-AMINO ACID DECARBOXYLASE-LIKE PROTEINS AND NUCLEIC ACIDS ENCODING SAME	LI, LI
<a href="#">60359944</a>	Not Issued	159	02/27/2002	L-SERINE DEHYDRATASE-LIKE PROTEINS, DERIVED PEPTIDES, AND NUCLEIC ACIDS ENCODING SAME	LI, LI
<a href="#">60348283</a>	Not Issued	159	11/09/2001	NOVEL HUMAN PROTEINS AND NUCLEIC ACIDS ENCODING SAME	LI, LI
<a href="#">60345221</a>	Not Issued	159	01/04/2002	NOVEL MAP KINASE-ACTIVATING DEATH DOMAIN PROTEIN-LIKE PROTEINS AND NUCLEIC ACIDS ENCODING SAME	LI, LI

<u>60343629</u>	Not Issued	159	10/24/2001	NOVEL HUMAN PROTEINS AND NUCLEIC ACIDS ENCODING SAME	LI, LI
<u>60341354</u>	Not Issued	159	12/14/2001	NOVEL UROPLAKIN 1B-LIKE PROTEINS AND NUCLEIC ACIDS ENCODING SAME	LI, LI
<u>60340225</u>	Not Issued	159	12/14/2001	NOVEL KETOHEXOKINASE-LIKE PROTEINS AND NUCLEIC ACIDS ENCODING SAME	LI, LI
<u>60338285</u>	Not Issued	159	12/07/2001	NOVEL HUMAN PROTEINS AND NUCLEIC ACIDS ENCODING SAME	LI, LI
<u>11095624</u>	Not Issued	018	03/31/2005	CNGH0011 POLYNUCLEOTIDES, POLYPEPTIDES, ANTIBODIES, AND COMPOSITIONS, AND METHODS OF PRODUCTION AND USE	LI, LI
<u>11087218</u>	Not Issued	020	03/23/2005	METHODS OF FORMING TRENCH ISOLATION IN THE FABRICATION OF INTEGRATED CIRCUITRY AND METHODS OF FABRICATING INTEGRATED CIRCUITRY	LI, LI
<u>11084616</u>	Not Issued	020	03/18/2005	SYSTEM AND METHOD FOR UTILIZING THE CONTENT OF AUDIO/VIDEO FILES TO SELECT ADVERTISING CONTENT FOR DISPLAY	LI, LI
<u>11079924</u>	Not Issued	019	03/14/2005	CAPACITOR STRUCTURE	LI, LI
<u>11077433</u>	Not Issued	020	03/10/2005	BIPHENYL COMPOUNDS USEFUL AS MUSCARINIC RECEPTOR ANTAGONISTS	LI, LI
<u>11076796</u>	Not Issued	020	03/10/2005	BIPHENYL COMPOUNDS USEFUL AS MUSCARINIC RECEPTOR ANTAGONISTS	LI, LI
<u>11076658</u>	Not Issued	020	03/10/2005	DIPHENYLMETHYL COMPOUNDS USEFUL AS MUSCARINIC RECEPTOR ANTAGONISTS	LI, LI
<u>11074099</u>	Not Issued	020	03/07/2005	SYSTEM AND METHOD FOR PROVIDING INSTANT MESSAGING CAPABILITY IN CONJUNCTION WITH AN ONLINE REFERENCE	LI, LI

<u>11072452</u>	Not Issued	020	03/07/2005	FORMATION OF MICRO LENS BY USING FLOWABLE OXIDE DEPOSITION	LI, LI
<u>11061821</u>	Not Issued	019	01/01/0001	METHODS AND COMPOSITIONS FOR TREATING IL-3 RELATED PATHOLOGIES	LI, LI
<u>11051724</u>	Not Issued	019	02/02/2005	THERAPEUTIC POLYPEPTIDES, NUCLEIC ACIDS ENCODING SAME, AND METHODS OF USE	LI, LI
<u>11044302</u>	Not Issued	030	01/28/2005	ANY GEAR START HORIZONTAL ENGINE FOR MOTORCYCLE	LI, LI
<u>11009282</u>	Not Issued	020	12/10/2004	METHODS OF ENHANCING SELECTIVITY OF ETCHING SILICON DIOXIDE RELATIVE TO ONE OR MORE ORGANIC SUBSTANCES; AND PLASMA REACTION CHAMBERS	LI, LI
<u>10999586</u>	Not Issued	020	11/30/2004	SYSTEMS AND METHODS FOR DETERMINING RELATIVE PLACEMENT OF CONTENT ITEMS ON A RENDERED PAGE	LI, LI
<u>10975720</u>	Not Issued	030	10/28/2004	EMBEDDED MULTILAYER PRINTED CIRCUIT	LI, LI
<u>10971479</u>	Not Issued	020	10/21/2004	NOVEL HUMAN PROTEINS AND POLYNUCLEOTIDES ENCODING THEM	LI, LI
<u>10024212</u>	Not Issued	161	12/18/2001	NOVEL PROTEINS AND NUCLEIC ACIDS ENCODING SAME	LI, LI
<u>09448556</u>	<u>6399504</u>	150	11/23/1999	METHODS AND ETCHANTS FOR ETCHING OXIDES OF SILICON WITH LOW SELECTIVITY	LI, LI
<u>09431812</u>	<u>6322954</u>	150	11/02/1999	WET INORGANIC AMMONIA ETCH OF ORGANICALLY MASKED SILICON-CONTAINING MATERIAL	LI, LI
<u>09430139</u>	<u>6271968</u>	150	10/29/1999	CUT-OFF FILTERS	LI, LI
<u>09383045</u>	<u>6306774</u>	150	08/25/1999	METHOD OF FORMING A WORDLINE	LI, LI
<u>09323749</u>	<u>6211054</u>	150	06/01/1999	METHOD OF FORMING A	LI, LI

				CONDUCTIVE LINE AND METHOD OF FORMING A LOCAL INTERCONNECT	
<u>09323464</u>	<u>6451127</u>	150	06/01/1999	CONDUCTIVE PASTE AND SEMICONDUCTOR COMPONENT HAVING CONDUCTIVE BUMPS MADE FROM THE CONDUCTIVE PASTE	LI, LI
<u>09305299</u>	<u>6241837</u>	150	05/05/1999	METHOD OF PRODUCING CERAMIC ARTICLE WITH RELIEF DECORATION	LI HO, LIN
<u>09293212</u>	<u>6194315</u>	150	04/16/1999	ELECTROCHEMICAL COBALT SILICIDE LINER FOR METAL CONTACT FILLS AND DAMASCENE PROCESSES	LI, LI
<u>09283666</u>	Not Issued	163	04/01/1999	PLATINUM POST-ETCH CLEAN DURING THE FORMATION OF A SEMICONDUCTOR DEVICE	LI, LI
<u>09283606</u>	<u>6459116</u>	150	04/01/1999	CAPACITOR STRUCTURE	LI, LI
<u>08556878</u>	<u>5825139</u>	150	11/02/1995	LAMP DRIVEN VOLTAGE TRANSFORMATION AND BALLASTING SYSTEM	LI LIN, LILY

Inventor Search Completed: No Records to Display.

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# **PALM INTRANET**

## Inventor Name Search Result

Your Search was:

Last Name = LI

First Name = WEIMIN

Application#	Patent#	Status	Date Filed	Title	Inventor Name 46
<a href="#">10991693</a>	Not Issued	030	11/18/2004	CVD OF PTRH WITH GOOD ADHESION AND MORPHOLOGY	LI, WEIMIN
<a href="#">10931355</a>	Not Issued	071	08/31/2004	PASSIVATION PROCESSES FOR USE WITH METALLIZATION TECHNIQUES	LI, WEIMIN
<a href="#">10916918</a>	Not Issued	030	08/12/2004	GAS DELIVERY SYSTEM FOR DEPOSITION PROCESSES, AND METHODS OF USING SAME	LI, WEIMIN
<a href="#">10913555</a>	Not Issued	041	08/06/2004	CHEMICAL TREATMENT OF SEMICONDUCTOR SUBSTRATES	LI, WEIMIN
<a href="#">10866290</a>	Not Issued	030	06/11/2004	METHOD OF IMPROVING HDP FILL PROCESS	LI, WEIMIN
<a href="#">10853063</a>	Not Issued	030	05/25/2004	METHOD OF ELIMINATING RESIDUAL CARBON FROM FLOWABLE OXIDE FILL	LI, WEIMIN
<a href="#">10806923</a>	Not Issued	030	03/22/2004	METHODS OF DEPOSITING SILICON DIOXIDE COMPRISING LAYERS IN THE FABRICATION OF INTEGRATED CIRCUITRY, METHODS OF FORMING TRENCH ISOLATION, AND METHODS OF FORMING ARRAYS OF MEMORY CELLS	LI, WEIMIN
<a href="#">10789736</a>	Not Issued	030	02/27/2004	TRANSPARENT AMORPHOUS CARBON STRUCTURE IN SEMICONDUCTOR DEVICES	LI, WEIMIN
<a href="#">10776553</a>	Not Issued	041	02/10/2004	COMPOSITIONS OF MATTER AND BARRIER LAYER COMPOSITIONS	LI, WEIMIN
<a href="#">10757638</a>	Not	094	01/13/2004	TECHNIQUE FOR HIGH	LI, WEIMIN

	Issued			EFFICIENCY METALORGANIC CHEMICAL VAPOR DEPOSITION	
<u>10756222</u>	Not Issued	041	01/13/2004	TECHNIQUE FOR HIGH EFFICIENCY METALORGANIC CHEMICAL VAPOR DEPOSITION	LI, WEIMIN
<u>10669671</u>	Not Issued	071	09/23/2003	METHODS OF FILLING GAPS AND METHODS OF DEPOSITING MATERIALS USING HIGH DENSITY PLASMA CHEMICAL VAPOR DEPOSITION	LI, WEIMIN
<u>10669667</u>	Not Issued	030	09/23/2003	ATOMIC LAYER DEPOSITION METHODS OF FORMING SILICON DIOXIDE COMPRISING LAYERS	LI, WEIMIN
<u>10661379</u>	Not Issued	041	09/12/2003	TRANSPARENT AMORPHOUS CARBON STRUCTURE IN SEMICONDUCTOR DEVICES	LI, WEIMIN
<u>10661100</u>	Not Issued	071	09/12/2003	MASKING STRUCTURE HAVING MULTIPLE LAYERS INCLUDING AN AMORPHOUS CARBON LAYER	LI, WEIMIN
<u>10642641</u>	6833605	150	08/19/2003	METHOD OF MAKING A MEMORY CELL CAPACITOR WITH TA2O5 DIELECTRIC	LI, WEIMIN
<u>10618220</u>	Not Issued	094	07/11/2003	METHODS FOR FILLING HIGH ASPECT RATIO TRENCHES IN SEMICONDUCTOR LAYERS	LI, WEIMIN
<u>10460624</u>	6866900	150	06/11/2003	DEPOSITION AND CHAMBER TREATMENT METHODS	LI, WEIMIN
<u>10435791</u>	Not Issued	071	05/12/2003	USE OF SPIN-ON, PHOTOPATTERNABLE, INTERLAYER DIELECTRIC MATERIALS AND INTERMEDIATE SEMICONDUCTOR DEVICE STRUCTURE UTILIZING THE SAME	LI, WEIMIN
<u>10420246</u>	Not Issued	092	04/21/2003	METHOD OF DEPOSITING A SILICON DIOXIDE COMPRISING LAYER DOPED WITH AT LEAST ONE OF P, B AND GE	LI, WEIMIN
<u>10419497</u>	Not	030	04/21/2003	3~6-DOF DECOUPLING	LI, WEIMIN

	Issued			STRUCTURE PARALLEL MICROMANIPULATOR	
<u>10357812</u>	Not Issued	061	02/04/2003	METHOD OF ELIMINATING RESIDUAL CARBON FROM FLOWABLE OXIDE FILL	LI, WEIMIN
<u>10338995</u>	6889141	150	01/10/2003	METHOD AND SYSTEM TO FLEXIBLY CALCULATE HYDRAULICS AND HYDROLOGY OF WATERSHEDS AUTOMATICALLY	LI, WEIMIN
<u>10319694</u>	6756293	150	12/16/2002	COMBINED GATE CAP OR DIGIT LINE AND SPACER DEPOSITION USING HDP	LI, WEIMIN
<u>10284681</u>	Not Issued	094	10/31/2002	GAS DELIVERY SYSTEM FOR DEPOSITION PROCESSES, AND METHODS OF USING SAME	LI, WEIMIN
<u>10234729</u>	6676756	150	08/30/2002	TECHNIQUE FOR HIGH EFFICIENCY METALORGANIC CHEMICAL VAPOR DEPOSITION	LI, WEIMIN
<u>10150843</u>	6777308	150	05/17/2002	METHOD OF IMPROVING HDP FILL PROCESS	LI, WEIMIN
<u>10137384</u>	Not Issued	092	05/03/2002	METHOD OF FABRICATING A SEMICONDUCTOR MULTILEVEL INTERCONNECT STRUCTURE	LI, WEIMIN
<u>10102110</u>	Not Issued	093	03/19/2002	LOW K INTERLEVEL DIELECTRIC LAYER FABRICATION METHODS	LI, WEIMIN
<u>10033656</u>	6835995	150	12/27/2001	LOW DIELECTRIC CONSTANT MATERIAL FOR INTEGRATED CIRCUIT FABRICATION	LI, WEIMIN
<u>10005439</u>	6573571	150	12/03/2001	SEMICONDUCTOR STRUCTURE INCLUDING METAL NITRIDE AND METAL SILICIDE LAYERS OVER ACTIVE AREA AND GATE STACK	LI, WEIMIN
<u>09629998</u>	6281072	150	08/01/2000	MULTIPLE STEP METHODS FOR FORMING CONFORMAL LAYERS	LI, WEIMIN
<u>09577835</u>	Not Issued	135	05/25/2000	PASSIVATION OF SIDEWALLS OF A WORD LINE STACK	LI, WEIMIN
<u>09537445</u>	Not Issued	168	03/27/2000	LOW K INTERLEVEL DIELECTRIC LAYER	LI, WEIMIN

				FABRICATION METHODS	
<u>09536037</u>	Not Issued	092	03/27/2000	LOW K INTERLEVEL DIELECTRIC LAYER FABRICATION METHODS	LI, WEIMIN
<u>09505608</u>	6472309	150	02/17/2000	IN SITU PLASMA PRE- DEPOSITION WAFER TREATMENT IN CHEMICAL VAPOR DEPOSITION TECHNOLOGY FOR SEMICONDUCTOR INTEGRATED CIRCUIT APPLICATIONS	LI, WEIMIN
<u>09388826</u>	Not Issued	061	09/01/1999	LOW K INTERLEVEL DIELECTRIC LAYER FABRICATION METHODS	LI, WEIMIN
<u>09388570</u>	6395647	150	09/02/1999	CHEMICAL TREATMENT OF SEMICONDUCTOR SUBSTRATES	LI, WEIMIN
<u>09376232</u>	6198144	150	08/18/1999	PASSIVATION OF SIDEWALLS OF A WORD LINE STACK	LI, WEIMIN
<u>09354572</u>	6368988	150	07/16/1999	COMBINED GATE CAP OR DIGIT LINE AND SPACER DEPOSITION USING HDP	LI, WEIMIN
<u>09200035</u>	6156674	150	11/25/1998	SEMICONDUCTOR PROCESSING METHODS OF FORMING INSULATIVE MATERIALS	LI, WEIMIN
<u>09146843</u>	6323101	150	09/03/1998	SEMICONDUCTOR PROCESSING METHODS, METHODS OF FORMING SILICON DIOXIDE, METHODS OF FORMING TRENCH ISOLATION REGIONS, AND METHODS OF FORMING INTERLEVEL DIELECTRIC LAYERS	LI, WEIMIN
<u>09076253</u>	6218288	150	05/11/1998	MULTIPLE STEP METHODS FOR FORMING CONFORMAL LAYERS	LI, WEIMIN
<u>09056309</u>	6372643	150	04/07/1998	METHOD FOR FORMING A SELECTIVE CONTACT AND LOCAL INTERCONNECT IN SITU AND SEMICONDUCTOR DEVICES CARRYING THE SAME	LI, WEIMIN
<u>09023523</u>	6136690	150	02/13/1998	IN SITU PLASMA PRE-	LI, WEIMIN



				DEPOSITION WAFER TREATMENT IN CHEMICAL VAPOR DEPOSITION TECHNOLOGY FOR SEMICONDUCTOR INTEGRATED CIRCUIT APPLICATIONS	
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Inventor Search Completed: No Records to Display.

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Day : Monday  
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Time: 10:20:25

**Inventor Name Search Result**

Your Search was:

Last Name = SANDHU

First Name = GURTEJ

Application#	Patent#	Status	Date Filed	Title	Inventor Name 49
<u>11027825</u>	Not Issued	020	12/29/2004	APPARATUS FOR FORMING THIN LAYERS OF MATERIALS ON MICRO-DEVICE WORKPIECES	SANDHU, GURTEJ
<u>10973343</u>	Not Issued	020	10/27/2004	STRUCTURALLY-STABILIZED CAPACITORS AND METHOD OF MAKING OF SAME	SANDHU, GURTEJ
<u>10669384</u>	Not Issued	030	09/24/2003	METHODS FOR FORMING CONDUCTIVE STRUCTURES AND STRUCTURES REGARDING SAME	SANDHU, GURTEJ
<u>10665151</u>	Not Issued	041	09/22/2003	STRUCTURALLY-STABILIZED CAPACITORS AND METHOD OF MAKING OF SAME	SANDHU, GURTEJ
<u>10615524</u>	Not Issued	092	07/03/2003	HAZE-FREE BST FILMS	SANDHU, GURTEJ
<u>10614489</u>	<u>6852593</u>	150	07/03/2003	HAZE-FREE BST FILMS	SANDHU, GURTEJ
<u>10614418</u>	Not Issued	094	07/03/2003	HAZE-FREE BST FILMS	SANDHU, GURTEJ
<u>10409145</u>	<u>6765250</u>	150	04/09/2003	SELF-ALIGNED, TRENCHLESS MAGNETORESISTIVE RANDOM-ACCESS MEMORY (MRAM) STRUCTURE WITH SIDEWALL CONTAINMENT OF MRAM STRUCTURE	SANDHU, GURTEJ
<u>10408450</u>	<u>6689624</u>	150	04/08/2003	METHOD OF FORMING SELF-ALIGNED, TRENCHLESS MAGNETORESISTIVE RANDOM-ACCESS MEMORY (MRAM) STRUCTURE WITH SIDEWALL CONTAINMENT OF MRAM STRUCTURE	SANDHU, GURTEJ

<u>10389910</u>	6835980	150	03/18/2003	SEMICONDUCTOR DEVICE WITH NOVEL FILM COMPOSITION	SANDHU, GURTEJ
<u>10175861</u>	Not Issued	071	06/21/2002	METHOD OF FORMING A NON-VOLATILE ELECTRON STORAGE MEMORY AND THE RESULTING DEVICE	SANDHU, GURTEJ
<u>10093394</u>	Not Issued	061	03/11/2002	VERSATILE ATOMIC LAYER DEPOSITION APPARATUS	SANDHU, GURTEJ
<u>10059308</u>	6596636	150	01/31/2002	ALD METHOD TO IMPROVE SURFACE COVERAGE	SANDHU, GURTEJ
<u>10039215</u>	Not Issued	071	01/03/2002	TOP ELECTRODE IN A STRONGLY OXIDIZING ENVIRONMENT	SANDHU, GURTEJ
<u>09982954</u>	Not Issued	120	10/22/2001	ATOMIC LAYER DOPING APPARATUS AND METHOD	SANDHU, GURTEJ
<u>09971945</u>	6660535	150	10/04/2001	METHOD OF FORMING HAZE-FREE BST FILMS	SANDHU, GURTEJ
<u>09785447</u>	6462313	150	02/20/2001	METHOD AND APPARATUS TO CONTROL TEMPERATURE IN AN RTP SYSTEM	SANDHU, GURTEJ
<u>09779219</u>	6395602	150	02/07/2001	METHOD OF FORMING A CAPACITOR	SANDHU, GURTEJ
<u>09716288</u>	6355561	150	11/21/2000	ALD METHOD TO IMPROVE SURFACE COVERAGE	SANDHU, GURTEJ
<u>09711206</u>	6534357	150	11/09/2000	METHODS FOR FORMING CONDUCTIVE STRUCTURES AND STRUCTURES REGARDING SAME	SANDHU, GURTEJ
<u>09653553</u>	6541353	150	08/31/2000	ATOMIC LAYER DOPING APPARATUS AND METHOD	SANDHU, GURTEJ
<u>09652863</u>	6682969	150	08/31/2000	TOP ELECTRODE IN A STRONGLY OXIDIZING ENVIRONMENT	SANDHU, GURTEJ
<u>09627649</u>	Not Issued	092	07/28/2000	INTERLEVEL DIELECTRIC STRUCTURE	SANDHU, GURTEJ
<u>09627381</u>	6841463	150	07/28/2000	INTERLEVEL DIELECTRIC STRUCTURE AND METHOD OF FORMING SAME	SANDHU, GURTEJ
<u>09570340</u>	Not Issued	041	05/12/2000	ATOMIC LAYER DEPOSITION APPARATUS	SANDHU, GURTEJ
<u>09495719</u>	6667502	150	02/01/2000	STRUCTURALLY-STABILIZED CAPACITORS AND METHOD OF MAKING OF SAME	SANDHU, GURTEJ

<u>09447981</u>	<u>6686288</u>	150	11/23/1999	INTEGRATED CIRCUIT HAVING SELF-ALIGNED CVD- TUNGSTEN/TITANIUM CONTACT PLUGS STRAPPED WITH METAL INTERCONNECT AND METHOD OF MANUFACTURE	SANDHU, GURTEJ
<u>09439944</u>	Not Issued	161	11/12/1999	METHOD FOR IN-SITU CLEANING OF INDUCTIVELY- COUPLED PLASMA CHAMBERS	SANDHU, GURTEJ
<u>09387775</u>	<u>6331379</u>	150	09/01/1999	IMPROVED PHOTOLITHOGRAPHY PROCESS USING MULTIPLE ANTI-REFLECTIVE COATINGS	SANDHU, GURTEJ
<u>09386316</u>	Not Issued	168	08/31/1999	STRUCTURALLY-STABILIZED CAPACITORS AND METHOD OF MAKING OF SAME	SANDHU, GURTEJ
<u>09382753</u>	<u>6319764</u>	150	08/25/1999	METHOD OF FORMING HAZE- FREE BST FILMS	SANDHU, GURTEJ
<u>09377273</u>	<u>6171943</u>	150	08/19/1999	METHODS OF FORMING A CONTACT HAVING TITANIUM SILICIDE FORMED BY CHEMICAL VAPOR DEPOSITION	SANDHU, GURTEJ
<u>09354572</u>	<u>6368988</u>	150	07/16/1999	COMBINED GATE CAP OR DIGIT LINE AND SPACER DEPOSITION USING HDP	SANDHU, GURTEJ
<u>09334753</u>	<u>6423626</u>	150	06/16/1999	REMOVAL OF METAL CUSP FOR IMPROVED CONTACT FILL	SANDHU, GURTEJ
<u>09267990</u>	<u>6380754</u>	150	03/12/1999	REMOVABLE ELECTRICAL INTERCONNECT APPARATUS INCLUDING AN ENGAGEMENT PROBE	SANDHU, GURTEJ
<u>09251387</u>	<u>6214687</u>	150	02/17/1999	METHOD OF FORMING A CAPACITOR AND A CAPACITOR CONSTRUCTION	SANDHU, GURTEJ
<u>09249659</u>	<u>6107686</u>	150	02/12/1999	INTERLEVEL DIELECTRIC STRUCTURE	SANDHU, GURTEJ
<u>09184489</u>	<u>5963832</u>	150	11/02/1998	REMOVAL OF METAL CUSP FOR IMPROVED CONTACT FILL	SANDHU, GURTEJ
<u>09146839</u>	<u>6727190</u>	150	09/03/1998	METHODS OF FORMING INSULATING MATERIALS	SANDHU, GURTEJ

<u>09041984</u>	<u>6455394</u>	150	03/13/1998	METHOD FOR TRENCH ISOLATION BY SELECTIVE DEPOSITION OF LOW TEMPERATURE OXIDE FILMS	SANDHU, GURTEJ
<u>08821936</u>	<u>5762537</u>	150	03/21/1997	SYSTEM FOR REAL-TIME CONTROL OF SEMICONDUCTOR WAFER POLISHING INCLUDING HEATER	SANDHU, GURTEJ
<u>08738789</u>	<u>5955758</u>	150	10/29/1996	METHOD OF FORMING A CAPACITOR PLATE AND A CAPACITOR INCORPORATING SAME	SANDHU, GURTEJ
<u>08631445</u>	<u>5789317</u>	150	04/12/1996	LOW TEMPERATURE REFLOW METHOD FOR FILLING HIGH ASPECT RATIO CONTACTS	SANDHU, GURTEJ
<u>08621157</u>	Not Issued	161	03/21/1996	METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR CIRCUITRY FOR OPERABILITY AND METHOD OF FORMING APPARATUS FOR TESTING SEMICONDUCTOR CIRCUITRY FOR OPERABILITY	SANDHU, GURTEJ
<u>08594842</u>	<u>5730835</u>	150	01/31/1996	FACET ETCH FOR IMPROVED STEP COVERAGE OF INTEGRATED CIRCUIT CONTACTS	SANDHU, GURTEJ
<u>08582385</u>	<u>6218237</u>	150	01/03/1996	METHOD OF FORMING A CAPACITOR	SANDHU, GURTEJ
<u>08572846</u>	<u>5959327</u>	150	12/14/1995	CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS HAVING A LOW CONTACT RESISTANCE LAYER AND THE METHOD FOR FORMING SAME	SANDHU, GURTEJ
<u>08512234</u>	<u>6040020</u>	150	08/07/1995	METHOD OF FORMING A FILM HAVING ENHANCED REFLOW CHARACTERISTICS AT LOW THERMAL BUDGET	SANDHU, GURTEJ

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117/89, 93, 95, 102

12/669, 667

### Examiner's Notes

SCAD or atomic (w) layer (w) deposit?  
 S (alter? or vary? or change for control? or adjust?) (8a) (flow? or slow? (6a) rate? or slow? (6a)  
 S (SiO<sub>2</sub> or silicon (w) dioxide)  
 S (substrate) (w) position? or placement?  
 S (flow?) (8a) (trimethylsilane)  
 S (chemisorb)  
 S (flow?) (8a) (oxidant #)  
 S (repeat?) (6a) (inventor as?)  
 S (first) and second  
 S (second) (6a) (inventor as?)

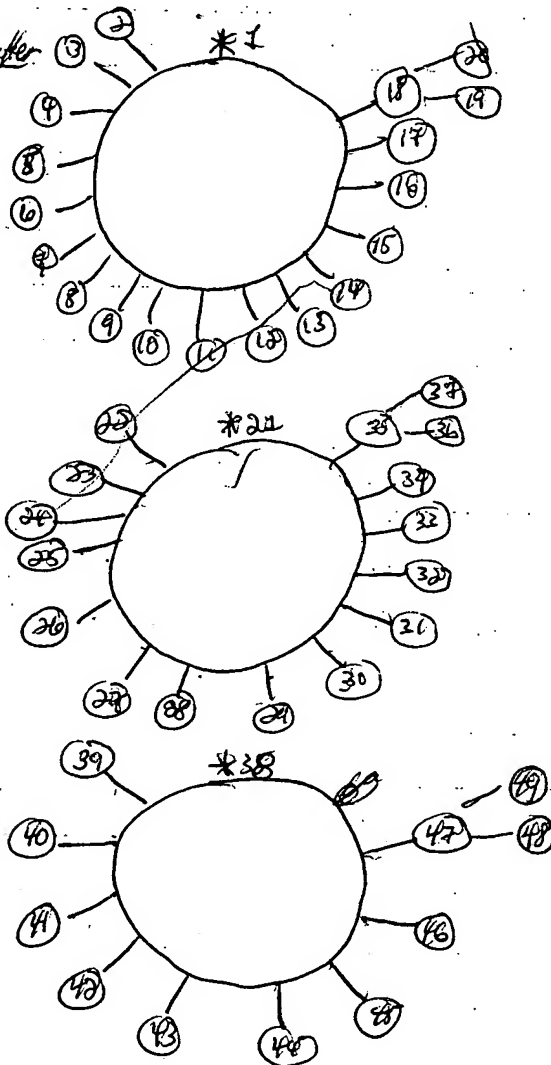
### Drawing 2 Object

In Fig 2, item #30 not mentioned in specification

### Allowable Subject Matter

~~Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100~~

11282 fig  
 claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100  
 "line 1, respectively  
 "trimethylsilane"  
 does not have proper  
 indentation



Search History

STN

(HCAPUS, INSPER, JAPPD, USPATFLL, INPADU)

5/23/05

=> d 111 1-5 abs, bib

L11 ANSWER 1 OF 5 USPATFULL on STN

AB A substrate is positioned within a deposition chamber.

**Trimethylsilane** is flowed to the chamber and a first inert gas is flowed to the chamber under conditions effective to chemisorb a first species monolayer comprising silicon onto the substrate. The first inert gas is flowed at a first rate. After forming the first species monolayer, an oxidant is flowed to the chamber and a second inert gas is flowed to the chamber under conditions effective to react the oxidant with the chemisorbed first species and form a monolayer comprising **silicon dioxide** on the substrate. The second inert gas flowing is at a second rate which is less than the first rate. The a) **trimethylsilane** and first inert gas flowing and the b) oxidant and second inert gas flowing are successively repeated effective to form a **silicon dioxide** comprising layer on the substrate. Other implementations and aspects are contemplated.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2005:71949 USPATFULL

TI **Atomic layer deposition** methods of forming **silicon dioxide** comprising layers

IN Li, Li, Meridian ID, UNITED STATES

Li, Weimin, Boise, ID, UNITED STATES

Sandhu, Gurtej S., Boise, ID, UNITED STATES

PI US 2005061234 A1 20050324

AI US 2003-669667 A1 20030923 (10)

DT Utility

FS APPLICATION

LREP WELLS ST. JOHN P.S., 601 W. FIRST AVENUE, SUITE 1300, SPOKANE, WA, 99201

CLMN Number of Claims: 49

ECL Exemplary Claim: 1

DRWN 1 Drawing Page(s)

LN.CNT 526

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L11 ANSWER 2 OF 5 USPATFULL on STN

AB One embodiment of the present invention is a cluster tool for processing wafers that includes: (a) one or more chemical vapor deposition chambers; (b) one or more e-beam treatment chambers; and (c) a transfer chamber adapted to transfer a wafer from one chamber to another while maintaining vacuum conditions.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:91974 USPATFULL

TI Cluster tool for E-beam treated films

IN Moghadam, Farhad, Saratoga, CA, UNITED STATES

Zhao, Jun, Cupertino, CA, UNITED STATES

Weidman, Timothy, Sunnyvale, CA, UNITED STATES

Roberts, Rick J., Sunnyvale, CA, UNITED STATES

Xia, Li-Qun, Santa Clara, CA, UNITED STATES

Demos, Alexandros T., Fremont, CA, UNITED STATES

PI US 2004069410 A1 20040415

AI US 2003-655276 A1 20030903 (10)

RLI Continuation of Ser. No. US 2003-428374, filed on 1 May 2003, PENDING

PRAI US 2002-378799P 20020508 (60)

DT Utility

FS APPLICATION

LREP PATENT COUNSEL, MS/2061, APPLIED MATERIALS, INC., Legal Affairs  
Department, P.O. Box 450A, Santa Clara, CA, 95052

CLMN Number of Claims: 14

ECL Exemplary Claim: 1

DRWN 8 Drawing Page(s)

LN.CNT 2658

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L11 ANSWER 3 OF 5 USPATFULL on STN

AB A method of forming (and apparatus for forming) refractory metal nitride layers (including silicon nitride layers), such as a tantalum nitride barrier layer, on a substrate by using an **atomic layer deposition** process (a vapor deposition process that includes a plurality of deposition cycles) with a refractory metal precursor compound, an organic amine, and an optional silicon precursor compound.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:57596 USPATFULL  
TI Systems and methods for forming refractory metal nitride layers using organic amines  
IN Vaartstra, Brian A., Nampa, ID, UNITED STATES  
PA MICRON TECHNOLOGY, INC., Boise, ID (U.S. corporation)  
PI US 2004043600 A1 20040304  
AI US 2002-229743 A1 20020828 (10)  
DT Utility  
FS APPLICATION  
LREP MUETING, RAASCH & GEBHARDT, P.A., P.O. BOX 581415, MINNEAPOLIS, MN, 55458  
CLMN Number of Claims: 55  
ECL Exemplary Claim: 1  
DRWN 2 Drawing Page(s)  
LN.CNT 1076

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L11 ANSWER 4 OF 5 USPATFULL on STM

AB One embodiment of the present invention is a method for fabricating a low-k dielectric film that includes steps of: (a) chemical vapor depositing a lower-k dielectric film; and (b) e-beam treating the lower-k dielectric film.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:330284 USPATFULL  
TI Methods and apparatus for E-beam treatment used to fabricate integrated circuit devices  
IN Moghadam, Farhad, Saratoga, CA, UNITED STATES  
Zhao, Jun, Cupertino, CA, UNITED STATES  
Weidman, Timothy, Sunnyvale, CA, UNITED STATES  
Roberts, Rick J., Sunnyvale, CA, UNITED STATES  
Xia, Li-Qun, Santa Clara, CA, UNITED STATES  
Demos, Alexandros T., Fremont, CA, UNITED STATES  
PI US 2003232495 A1 20031218  
AI US 2003-428374 A1 20030501 (10)  
PRAI US 2002-378799P 20020508 (60)  
DT Utility  
FS APPLICATION  
LREP PATENT COUNSEL, MS/2061, APPLIED MATERIALS, INC., Legal Affairs Department, P.O.Box 450A, Santa Clara, CA, 95052  
CLMN Number of Claims: 22  
ECL Exemplary Claim: 1  
DRWN 8 Drawing Page(s)  
LN.CNT 2666

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L11 ANSWER 5 OF 5 USPATFULL on STM

AB A method for forming a metal interconnect on a substrate is provided. In one aspect, the method comprises depositing a refractory metal containing barrier layer having a thickness that exhibits a crystalline like structure and is sufficient to inhibit atomic migration on at least a portion of a metal layer by alternately introducing one or more pulses of a metal-containing compound and one or more pulses of a nitrogen-containing compound; depositing a seed layer on at least a portion of the barrier layer; and depositing a second metal layer on at least a portion of the seed layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:180434 USPATFULL  
TI Integration of **ALD** tantalum nitride and alpha-phase tantalum



for copper metallization application

IN Chen, Ling, Sunnyvale, CA, UNITED STATES  
 Chung, Hua, San Jose, CA, UNITED STATES  
 Seutter, Sean M., San Jose, CA, UNITED STATES  
 Yang, Michael X., Palo Alto, CA, UNITED STATES  
 Xi, Ming, Palo Alto, CA, UNITED STATES  
 Ku, Vincent, San Jose, CA, UNITED STATES  
 Wu, Dien-Yeh, San Jose, CA, UNITED STATES  
 Ouye, Alan, San Mateo, CA, UNITED STATES  
 Nakashima, Norman, Sunnyvale, CA, UNITED STATES  
 Chin, Barry, Saratoga, CA, UNITED STATES  
 Zhang, Hong, Fremont, CA, UNITED STATES

PI US 2003124262 A1 20030703  
 AI US 2002-281386 A1 20021025 (10)  
 PRAI US 2001-346086P 20011026 (60)  
 DT Utility  
 FS APPLICATION  
 LREP APPLIED MATERIALS, INC., PATENT COUNSEL, Legal Affairs Department, P.O.  
 BOX 450A, Santa Clara, CA, 95052  
 CLMN Number of Claims: 19  
 ECL Exemplary Claim: 1  
 DRWN 6 Drawing Page(s)  
 LN.CNT 1034  
 CAS INDEXING IS AVAILABLE FOR THIS PATENT

=> d his

(FILE 'HOME' ENTERED AT 10:01:24 ON 23 MAY 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC' ENTERED AT  
 10:02:21 ON 23 MAY 2005

L1 20410 S (ALD OR ATOMIC(W)LAYER(W)DEPOSIT? OR ALE OR ATOMIC(W)LAYER(W)  
 L2 869964 S (ALTER? OR VARY? OR CONTROL? OR DIFFER? OR ADJUST?) (8A) (FLOW?  
 L3 564469 S (SIO2 OR SILICON(W)DIOXIDE)  
 L4 6919 S (TRIMETHYLSILANE)  
 L5 29782 S (CHEMISORB?)  
 L6 4319 S (FLOW?) (6A) (OXIDANT#)  
 L7 2936 S (FIRST) (4A) (INERT(W)GAS?)  
 L8 2929 S (SECOND?) (4A) (INERT(W)GAS?)  
 L9 1 S L1 AND L2 AND L3 AND L4 AND L6 AND L7 AND L8  
 L10 1 S L1 AND L2 AND L3 AND L4 AND L6  
 L11 5 S L1 AND L2 AND L3 AND L4

=>

=> d his

(FILE 'HOME' ENTERED AT 10:01:24 ON 23 MAY 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC' ENTERED AT  
10:02:21 ON 23 MAY 2005

L1 20410 S (ALD OR ATOMIC(W) LAYER(W) DEPOSIT? OR ALE OR ATOMIC(W) LAYER(W)  
L2 869964 S (ALTER? OR VARY? OR CONTROL? OR DIFFER? OR ADJUST?) (8A) (FLOW?  
L3 564469 S (SIO2 OR SILICON(W) DIOXIDE)  
L4 6919 S (TRIMETHYLSILANE)  
L5 29782 S (CHEMISORB?)  
L6 4319 S (FLOW?) (6A) (OXIDANT#)  
L7 2936 S (FIRST) (4A) (INERT(W) GAS?)  
L8 2929 S (SECOND?) (4A) (INERT(W) GAS?)

=> s l1 and l2 and l3 and l4 and l6 and l7 and l8

L9 1 L1 AND L2 AND L3 AND L4 AND L6 AND L7 AND L8

=> d l9 abs,bib

L9 ANSWER 1 OF 1 USPATFULL on STN

AB A substrate is positioned within a deposition chamber.  
**Trimethylsilane** is flowed to the chamber and a **first inert gas** is flowed to the chamber under conditions effective to chemisorb a first species monolayer comprising silicon onto the substrate. The **first inert gas** is flowed at a **first rate**. After forming the first species monolayer, an **oxidant** is flowed to the chamber and a **second inert gas** is flowed to the chamber under conditions effective to react the oxidant with the chemisorbed first species and form a monolayer comprising **silicon dioxide** on the substrate. The **second inert gas** flowing is at a **second rate** which is less than the first rate. The a) **trimethylsilane** and **first inert gas** flowing and the b) **oxidant** and **second inert gas** flowing are successively repeated effective to form a **silicon dioxide** comprising layer on the substrate. Other implementations and aspects are contemplated.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2005:71949 USPATFULL

TI **Atomic layer deposition** methods of forming  
**silicon dioxide** comprising layers

IN Li, Li, Meridian, ID, UNITED STATES

Li, Weimin, Boise, ID, UNITED STATES

Sandhu, Gurtej S., Boise, ID, UNITED STATES

PI US 2005061234 A1 20050324

AI US 2003-669667 A1 20030923 (10)

DT Utility

FS APPLICATION

LREP WELLS ST. JOHN P.S., 601 W. FIRST AVENUE, SUITE 1300, SPOKANE, WA, 99201

CLMN Number of Claims: 49

ECL Exemplary Claim: 1

DRWN 1 Drawing Page(s)

LN.CNT 526

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

=> d 16 1-5 abs,bib

L6 ANSWER 1 OF 5 USPATFULL on STN

AB A substrate is positioned within a deposition chamber.  
**Trimethylsilane** is flowed to the chamber and a first inert gas is flowed to the chamber under conditions effective to chemisorb a first species monolayer comprising silicon onto the substrate. The first inert gas is flowed at a first rate. After forming the first species monolayer, an oxidant is flowed to the chamber and a second inert gas is flowed to the chamber under conditions effective to react the oxidant with the chemisorbed first species and form a monolayer comprising **silicon dioxide** on the substrate. The second inert gas flowing is at a second rate which is less than the first rate. The a) **trimethylsilane** and first inert gas flowing and the b) oxidant and second inert gas flowing are successively repeated effective to form a **silicon dioxide** comprising layer on the substrate.  
Other implementations and aspects are contemplated.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2005:71949 USPATFULL  
TI **Atomic layer deposition** methods of forming  
**silicon dioxide** comprising layers  
IN Li, Li, Meridian, ID, UNITED STATES  
Li, Weimin, Boise, ID, UNITED STATES  
Sandhu, Gurtej S., Boise, ID, UNITED STATES  
PI US 2005061234 A1 20050324  
AI US 2003-669667 A1 20030923 (10)  
DT Utility  
FS APPLICATION  
LREP WELLS ST. JOHN P.S., 601 W. FIRST AVENUE, SUITE 1300, SPOKANE, WA, 99201  
CLMN Number of Claims: 49  
ECL Exemplary Claim: 1  
DRWN 1 Drawing Page(s)  
LN.CNT 526

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L6 ANSWER 2 OF 5 USPATFULL on STN

AB One embodiment of the present invention is a cluster tool for processing wafers that includes: (a) one or more chemical vapor deposition chambers; (b) one or more e-beam treatment chambers; and (c) a transfer chamber adapted to transfer a wafer from one chamber to another while maintaining vacuum conditions.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:91974 USPATFULL  
TI Cluster tool for E-beam treated films  
IN Moghadam, Farhad, Saratoga, CA, UNITED STATES  
Zhao, Jun, Cupertino, CA, UNITED STATES  
Weidman, Timothy, Sunnyvale, CA, UNITED STATES  
Roberts, Rick J., Sunnyvale, CA, UNITED STATES  
Xia, Li-Qun, Santa Clara, CA, UNITED STATES  
Demos, Alexandros T., Fremont, CA, UNITED STATES  
PI US 2004069410 A1 20040415  
AI US 2003-655276 A1 20030903 (10)  
RLI Continuation of Ser. No. US 2003-428374, filed on 1 May 2003, PENDING  
PRAI US 2002-378799P 20020508 (60)  
DT Utility  
FS APPLICATION  
LREP PATENT COUNSEL, MS/2061, APPLIED MATERIALS, INC., Legal Affairs  
Department, P.O. Box 450A, Santa Clara, CA, 95052  
CLMN Number of Claims: 14  
ECL Exemplary Claim: 1  
DRWN 8 Drawing Page(s)  
LN.CNT 2658

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L6 ANSWER 3 OF 5 USPATFULL on STN

AB A method of forming (and apparatus for forming) refractory metal nitride

layers (including silicon nitride layers), such as a tantalum nitride barrier layer, on a substrate by using an **atomic layer deposition** process (a vapor deposition process that includes a plurality of deposition cycles) with a refractory metal precursor compound, an organic amine, and an optional silicon precursor compound.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:57596 USPATFULL  
TI Systems and methods for forming refractory metal nitride layers using organic amines  
IN Vaartstra, Brian A., Nampa, ID, UNITED STATES  
PA MICRON TECHNOLOGY, INC., Boise, ID (U.S. corporation)  
PI US 2004043600 A1 20040304  
AI US 2002-229743 A1 20020828 (10)  
DT Utility  
FS APPLICATION  
LREP MUETING, RAASCH & GEBHARDT, P.A., P.O. BOX 581415, MINNEAPOLIS, MN, 55458  
CLMN Number of Claims: 55  
ECL Exemplary Claim: 1  
DRWN 2 Drawing Page(s)  
LN.CNT 1076

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L6 ANSWER 4 OF 5 USPATFULL on STN  
AB One embodiment of the present invention is a method for fabricating a low-k dielectric film that includes steps of: (a) chemical vapor depositing a lower-k dielectric film; and (b) e-beam treating the lower-k dielectric film.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:330284 USPATFULL  
TI Methods and apparatus for E-beam treatment used to fabricate integrated circuit devices  
IN Moghadam, Farhad, Saratoga, CA, UNITED STATES  
Zhao, Jun, Cupertino, CA, UNITED STATES  
Weidman, Timothy, Sunnyvale, CA, UNITED STATES  
Roberts, Rick J., Sunnyvale, CA, UNITED STATES  
Xia, Li-Qun, Santa Clara, CA, UNITED STATES  
Demos, Alexandros T., Fremont, CA, UNITED STATES  
PI US 2003232495 A1 20031218  
AI US 2003-428374 A1 20030501 (10)  
PRAI US 2002-378799P 20020508 (60)  
DT Utility  
FS APPLICATION  
LREP PATENT COUNSEL, MS/2061, APPLIED MATERIALS, INC., Legal Affairs Department, P.O.Box 450A, Santa Clara, CA, 95052  
CLMN Number of Claims: 22  
ECL Exemplary Claim: 1  
DRWN 8 Drawing Page(s)  
LN.CNT 2666

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L6 ANSWER 5 OF 5 USPATFULL on STN  
AB A method for forming a metal interconnect on a substrate is provided. In one aspect, the method comprises depositing a refractory metal containing barrier layer having a thickness that exhibits a crystalline like structure and is sufficient to inhibit atomic migration on at least a portion of a metal layer by alternately introducing one or more pulses of a metal-containing compound and one or more pulses of a nitrogen-containing compound; depositing a seed layer on at least a portion of the barrier layer; and depositing a second metal layer on at least a portion of the seed layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:180434 USPATFULL  
TI Integration of **ALD** tantalum nitride and alpha-phase tantalum for copper metallization application

IN Chen, Ling, Sunnyvale, CA, UNITED STATES  
Chung, Hua, San Jose, CA, UNITED STATES  
Seutter, Sean M., San Jose, CA, UNITED STATES  
Yang, Michael X., Palo Alto, CA, UNITED STATES  
Xi, Ming, Palo Alto, CA, UNITED STATES  
Ku, Vincent, San Jose, CA, UNITED STATES  
Wu, Dien-Yeh, San Jose, CA, UNITED STATES  
Ouye, Alan, San Mateo, CA, UNITED STATES  
Nakashima, Norman, Sunnyvale, CA, UNITED STATES  
Chin, Barry, Saratoga, CA, UNITED STATES  
Zhang, Hong, Fremont, CA, UNITED STATES  
PI US 2003124262 A1 20030703  
AI US 2002-281386 A1 20021025 (10)  
PRAI US 2001-346086P 20011026 (60)  
DT Utility  
FS APPLICATION  
LREP APPLIED MATERIALS, INC., PATENT COUNSEL, Legal Affairs Department, P.O.  
BOX 450A, Santa Clara, CA, 95052  
CLMN Number of Claims: 19  
ECL Exemplary Claim: 1  
DRWN 6 Drawing Page(s)  
LN.CNT 1034  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

=> d his

(FILE 'HOME' ENTERED AT 10:42:04 ON 23 MAY 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC' ENTERED AT  
10:42:26 ON 23 MAY 2005

L1 20410 S (ALD OR ATOMIC(W)LAYER(W)DEPOSIT? OR ALE OR ATOMIC(W)LAYER(W)  
L2 564469 S (SIO2 OR SILICON(W)DIOXIDE)  
L3 6919 S (TRIMETHYLSILANE)  
L4 24 S L1 AND L2 AND L3  
L5 875677 S (ALTER? OR VARY? OR DIFFER? OR ADJUST? OR CONTROL?) (8A) (FLOW?  
L6 5 S L4 AND L5

=>